

Tanner Tools v15.12

Release Notes

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Tanner Tools Version 15.12

What's New in S-Edit v15.12

- The S-Edit Print dialog now has an option to turn on Evaluated Properties for printing. The option is "ON" by default.

Bug Fixes

- S-Edit now offers to save work when the machine is shutdown or when logging off from a remote machine.
- When instancing a cell and modifying a property value, the modified value is now correctly used.
- The order of a bus is now written correctly in Verilog Output.
- The values of 'device name', 'type', and 'region' in the Small-signal Parameters dialog are now displayed correctly.
- The value of the Monte parameter in **Setup Spice Simulation > Transient/Fourier Analysis** is now saved.
- Setting the page size for a schematic specific view now works for cells in any level of the design.
- Fixed problem in Spice import in handling of node names with backslash character.
- Fixed problem in parsing of SW is a voltage-controlled switch, which was leading to incorrect ports being added to the interface view.
- S-Edit now detects an infinite recursion in an expression, and outputs an empty string as a result.
- Fixed problem in copy/paste of Spice property trees.
- Generating a symbol no longer requires extracting a netlist first.

What's New in T-Spice v15.12

Bug Fixes

- Print expressions involving more than one noise source reference were wrong. e.g. `.print noise 'dn(M1,ID)+dn(M1,FN)'`
- Performance improvements have been made for simulations with large amounts of output, such as using `.probe` for a circuit with tens or hundreds of thousands of nodes.
- Added VC1R and VC2R coefficients to resistor models for simulating voltage dependent resistances.
- As a performance and convergence enhancement, devices with all terminals floating (unattached to other devices) will be ignored.
- Corrected VBIC transistor scaling due to M, area, or Scale device parameters which was incorrect for models using `td` excess phase term.
- Removed the PSP 102.1 model due to bugs in the vendor-supplied code. PSP 102.0 or 103.0 are used instead.
- Corrected problems under certain circumstances when the `tnom` model parameter could be incorrect.
- Corrected some format issues with Spice raw file output (`.options nutmeg`).

What's New in W-Edit v15.12

- **Note:** In order to make performance improvements in W-Edit and T-Spice, the simulation database written by T-Spice v15.12 is not backward compatible.

Simulation results written by T-Spice v15.12 will not load into W-Edit v15.11 and prior.

- The number of significant digits displayed on axis and cursor tables may now be configured. Default settings for all charts may be set in the **Setup > Chart Styles** dialog, and for a specific chart may be set by right clicking on the chart and choosing **Chart Properties**.
- **File > Export Chart Data...** now writes 12 significant digits when exporting data.
- Cursor and marker names can now be used in measurements whenever an $-x$ value or a $-y$ value is needed.
- the “calc $-tcl$ ” command now returns a list of points, rather than a list of lists when the expression in the command returns is a measurement that returns only one point per variation.

Bug Fixes

- **File > Export Chart Data ...** now exports AC traces correctly.
- Vertical Pan now pans all plots when no curves are selected.
- Fixed crash in W-Edit that occurred while panning with a cursor selected.
- Improved performance of FFT function. This was causing databases that used FFTs to take a long time to open.

What's New in L-Edit Pro v15.12

- The Mouse Wheel behavior is now configurable in **Setup > Application > Mouse**. The default behavior can be setup to Zoom-In, Zoom-Out, or Pan-Vertical. Pressing the Ctrl key switches the wheel behavior between panning and zooming, and pressing the Shift key switches behavior between Pan-Vertical and Pan-Horizontal. These also work while drawing an object.
- The layer selector in the Edit Object Dialog now lists only the layers that are shown in the layer palette.
- Added a new struct called LLayerParamEx1512, which adds a new member to the struct LLayerParamEx830 to indicate the protected status of a layer. New functions LLayer_GetParametersEx1512, and LLayer_SetParametersEx1512 are added. If a layer is Protected, it is not selectable.

Bug Fixes

- Fixed a problem where L-Edit GUI would pause for about a second every 150 seconds.
- Fixed a problem in Snap to vertex while editing an edge. Also fixed problem in some circumstances when both edge and vertex snapping are on, edge would take priority.
- Crash when Ctrl + Middle Scroll when Design Navigator is in focus is fixed.
- Snap now works when performing a Nibble operation.
- Fixed a slowdown in Generate layers.

What's New in HiPer Verify v15.12

- Parsing of Calibre DRC files no longer flags ERC MAXIMUM VERTEX as a syntax error.
- Fixed a problem in parsing of Calibre files that gave “Error parsing .tdr file”.
- Width and spacing violations on all 45 and angle geometry that in some conditions were missed, are now correctly found.
- Fixed missing violations when PERPENDICULAR ALSO option is used with EXT command.
- Fixed false errors found on hierarchical layout that were not found on flat layout.

Tanner Tools Version 15.11

What's New in S-Edit v15.11

- Import Spice now has two options, i) "Parse Connectivity" , and ii) "Preserve Text". The "Parse Connectivity" option will parse the connectivity from a Spice netlist, including files that are referenced by .include statements. Spice views are then auto-generated from the connectivity views. The "Preserve Text" option copies the text verbatim for each subcircuit in the input Spice file, as well as the toplevel, into separate subcircuits, and does not follow into .include files.
- Import Verilog now has two options, i) "Parse Connectivity (Structural Verilog)", and ii) "Preserve Text (Verilog-A)". The "Parse Connectivity" option will parse the connectivity from a Verilog netlist, the connectivity is then displayed as Spice views that are auto-generated from the connectivity views. The "Preserve Text" option copies the text verbatim for each subcircuit in the input Verilog file, as well as the toplevel, into separate subcircuits. This is useful for importing a library of definitions that are all in one file.
- Probing Small Signal Parameters is now working.
- Starting a simulation while pushed into a subcell in the hierarchy now works correctly.
- Verilog import now creates pins in the correct order in SPICE.PINORDER.
- Fixed problem where empty schematic views would be created for primitive devices after importing Spice, then saving and reopening design.
- Traces now properly obey Trace Style Settings.
- Fixed problem with "se" function introduced in v15.10 where "se a b c" would return "c" instead of the correct second argument "b". This was resulting in incorrect parameter values being written to Spice when this form of "se" was used.
- Fixed problem with evaluation of ValidValues sub-property, which could result in incorrect parameter values exported to Spice if the ValidValues sub-property was used.

What's New in T-Spice v15.11

- The **.load** command now issues a warning rather than an error if the input file is not found. This enables use of **.save** and **.load** in the same file, so that repeated runs may be faster by restoring previously computed operating point values.
- Made corrections to the corner rounding effects of Pulse and PWL source waveform Round=r parameter.
- A warning will now be issued if a directory listed in **.option search=...** does not exist.
- Corrected **.measure** operations involving derivative functions (ddt, ddx, etc.) which were erroneously resulting in 'not found' solutions.
- Corrected the **.measure autostop** feature, which was not stopping the transient simulation under certain circumstances involving multiple measurements.
- Made corrections to the VBIC power calculations
- Fixed parsing of inline comment immediately following a closing single quote, as in **.PARAM CjN='1.5E-3'\$This is a test.**
- Performance of T-Spice is improved in cases where large amounts of text are written to the output window.
- Inline comments may now begin with an asterisk (*) as well as the previously supported dollar sign (\$).
- Added support for g element VCR voltage-controlled resistor syntax.
- New option, **monteinfo={0,1,2}**, controls what outputs are generated during Monte Carlo analysis. The default value, 1, displays all statistical information and measurement results. You should set **monteinfo=2** to additionally get all plot results for each monte carlo variation.

What's New in W-Edit v15.11

- Saving **Setup > Chart Styles** when in non-English translation setting is now fixed.
- Units can now be specified in the calc and trace define commands by adding -units xxx, -xunits xxx, or -yunits xxx, where xxx is the name of a unit. The list of units can be obtained by entering measure units on the command line.
- Fixed “find maximum” and “find minimum” commands for AC charts by first computing the magnitude or phase of the complex trace inside the amax command. Also modified the “Chart” button on the waveform calculator to compute the magnitude or phase of the complex trace when inserting the trace name from an AC chart.
- Fixed crash when hiding traces from the Trace Navigator.

What's New in L-Edit Pro v15.11

Snapping to Wire Centerlines

- Object Snapping now is now able to snap to the edge of wires. Edge snapping now snaps to wires edges, and Center snapping snaps to circle and rectangle centers and wire centerlines.
- Paste to cursor of instances now places the cursor at the origin of the instance rather than at the center of the instance. If the origin of the instance is outside the instance boundary, then the cursor is placed at the closest corner of the instance boundary to the origin.

UPI

New UPI functions are added to get and set the current layer palette, to get the name of the net layer palette, and to create or overwrite a layer palette.

Bug Fixes

- Incorrect gaps and overlaps in **Tools > Add-Ins > Layer Fill** command have been fixed. Also, the temporary layer “LayerFillScratch” is now deleted upon completion of the Layer Fill command.
- Error when generating Guard Ring with layers hidden has been fixed.
- Fixed problem where Contacts defined in v15.02 or prior were not transferred into v15.10.

What's New in HiPer Verify v15.11

- Problem with DRC distances incorrectly displayed as {0} in the Verification Error Navigator is fixed.
- Missing DRC errors in certain 45 and all-angle geometry are now correctly flagged.
- Fixed internal error in Standard Extract when layer alias optimization caused the device recognition layer and all pin layers to be the same.
- Fixed bug in Extract where results were different extracting hierarchical vs flat layout in certain conditions.
- Fixed problem with false errors in Net Area Ratio command.
- Fixed crash in DRC on SIZE operation on certain geometry.

Tanner Tools Version 15.10

What's New in S-Edit v15.10

Improvements in Bus, Port, and Netname Processing

- If multiple buses (with different dimension) connect to a single net, S-Edit will now connect all the buses to this single net. Prior to v15.10 this would be an error due to the connection of busses with different dimension.
- When a net label is placed on a pin connectivity will now be correctly extracted.
- A ports on a symbol can now connect to netlabel or port with the same name on the schematic. Previously a port on a symbol could only connect to a port on the schematic.

Improvements in Spice, EDIF, and Verilog Import

- Spice, EDIF, and Verilog import will now create Spice views. Since Spice views are saved with the design, the imported Spice will be saved. In v15.02 and prior versions, Spice import would only create connectivity views, but connectivity views are not saved, so the imported spice would be lost on saving. Importing a hierarchical netlist will create separate cells for each subcircuit in the netlist.

Improved Control of Write Permissions

- Improved control over write permissions has been established. When opening a design, you can now choose to attempt to open the design with Exclusive or Non-Exclusive access. Opening a design with **Exclusive Access** means reserving the right to save a design, so that no-one else can write to it while you have it open. This “write reservation” gives you the exclusive right to save a design. Opening a design with **Non-Exclusive Access** means you *might* be able to write to the design in the future, as long as no one else secures a write reservation before you attempt to save the design.

Corner Simulations

- Corner Simulations can now be setup in the S-Edit Setup **Spice Simulation** dialog. Parameters, Temperature, and libraries may be set to any value for each corner that is defined.

Corner Simulation and Other New Simulation Settings

- The Setup Simulation dialog now supports a new sweep type for Monte Carlo simulation in Transient, AC, DC, and Parameter Sweep analysis. A new List capability has been added in DC and Parameter Sweep analysis, adding to the List ability that already existed in AC and Temperature sweeps.
- Setup Simulation > Transient/Fourier Analysis now has the "npoints" and "interpolate" parameters. These are the “Fourier Number of Points” and “Interpolate Data Points” fields in the dialog.

Probing Buses

- When probing a bus, multiple (or all) signals can now be selected for probing. Previously only a single signal in the bus could be selected for probing.

Other Improvements

- The “Save Design and it's libraries” command has been renamed to “Save all changes”. This command saves all design and library components that have changed. The “Save Selected Design/Libraries” will force a save of the selected Design/Libraries. Note that if a design or library is marked “No Edit” then the attempt to save will be aborted. Also, if a design/library is locked by another user, it will not be saved.
- By default, unnamed nets in S-Edit are given names like N_1, N_2... A. Tcl variable "tanner_unnamednetprefix" can now be assigned with a value which replaces the default prefix ("N_") with the user supplied prefix.

Bug Fixes

- Fixed a problem where adding a library which includes other sub libraries to a design and then saving the design, would result in the contents of the libraries.lst file being erased.
- Fixed crash when removing an unresolved library and then adding a new library.
- Fixed a problem on EDIF import, where ports were sometimes not rotated correctly.
- Fixed a bug in Copy Cell command to no longer automatically change the cell name when a different design is chosen, as this had the possibility of unintentionally overwriting an existing cell.
- Symbol update will now place properties on symbol if symbol is being generated from interface, ie there is no schematic.
- Export to flat Spice as subcircuit now correctly puts subcircuit wrapper around the netlist.
- Fixed problem where the space after the net name was missing, if a net ended in a plus sign, causing two net names to be combined into one.
- Rename Property now works. To rename a property, select the property on the schematic/symbol page, then right-click on the property name at the top of the property browser, and select “Rename Property”.
- S-Edit does not allow instancing from a primary design into a library. S-Edit will now warn on EDIF import if this will occur, and will not allow the import. To be able to import in this situation, one should choose a different design name for the design into which the import is done.
- Fixed a problem where in certain cases S-Edit was exporting EDIF with empty property values.

What's New in T-Spice v15.10

Updated Models

- Updated the BSIM4-SOI transistor model to the latest Berkeley version 4.3 release.
- Updated the BSIM4 transistor model to the latest Berkeley version 4.6.5 release.
- Modified the PSP model level to be 69, to match HSPICE and foundry model conventions.
- Updated Philips SiMKit to release 3.4 with the latest Mos11, Mextram, PSP, and other models.

Improved Performance

- Improved the performance of simulations involving expression-controlled devices, such as behavioral resistors, capacitors, and VCCS elements.

Other Improvements

- Updated the Verilog-A compiler and interface to include a number of new features and bug fixes.
- The T-Spice User Interface has been improved with several new commands available in the Simulation Manager window for opening and comparing solution files, and renaming or deleting simulation results.
- **.measure** command outputs are now stored to a file, *.meas, as well as being printed to the simulation log.
- Added a new option **measinfo = 0,1** (default=0) to control what outputs are generated for the **.measure** command. 0 is for minimal output (measured value only). 1 is for added outputs: at, when, from, to, etc. intermediate values.
- **.measure** command results can now be tested with the **.assert** command using the **measure=measurename** argument.
- Added a new test feature to the **.assert** command; the **value=v** argument will test for value equality.
- The expression calculator supports a new **random(max)** function which will return a random number between 0 and max.
- Improved the **.del lib** command so that the the library name can differ from the original **.lib** library name, so long as the actual file is the same. e.g. one command can use a relative path name, the other an absolute path, and the **.del lib** command will work.
- Improved the error handling and message when a simulation fails because an output file is write-protected.
- Removed some limitations for user-defined functions when used in plot statements; arguments to the functions may now be any plot item, noise value, etc.
- Corrected problems with user-defined functions which under certain circumstances could not evaluate **.param** values in the equation.
- Corrected erroneous data that was plotted for time 0 to time s, when the **.tran ... start=s** command is used together with **.option prtdel=d**.
- Added the ability to plot a number of switch device state variables: Vc, Vr, Ic, R, Power.
- Added an optional initial condition flag [ON|OFF] (default value: off) for switch devices.
- New **.title** title command allows you to create a simulation title for display in log outputs and plots. The **.title** command also names the base **.alter** in the W-Edit simulations browser.
- The default **bytol** option value has changed from 1e-9 to 1e-12 to improve accuracy with slightly degraded performance.
- The expression calculator will now properly determine the value of a variable named **j#** (e.g. **.param j1=...**) rather than always processing it as an imaginary number (e.g. complex 0 + j1).
- Modified the **.param** evaluation rules so that if a parameter is defined more than once, the final definition will be used rather than the first.
- Corrected some DC sweep convergence problems.
- Corrected a Monte Carlo variable listing problem that showed numerous 'unknown variable' entries.

Bug Fixes

- Corrected a Philips SiMKit bug which affected the PSP PMOS model sign conventions.
- Fixed a crash bug when Philips SiMKit models (MOS11, PSP, Mextram, etc.) are defined and repeatedly used in subcircuits.
- Fixed a crash bug when performing noise analysis on Verilog-A devices.

- Corrected capacitor and resistor error checking to issue an error if the device instance specifies both a model and a capacitance/resistance value, and the model does not exist. Previously, the missing model definition was silently ignored.

What's New in W-Edit v15.10

Histogram Charts

- A new Histogram chart type is now available in W-Edit. Results of .MEASURE commands in a Monte Carlo simulation are now automatically plotted on a histogram upon completion of the simulation.

Eye Diagrams

- A new Eye diagrams chart type is now available in W-Edit. Create a new Chart using the **Chart > New Chart** command, and then add a trace to the chart.

Chart Setup

- Background, margin, grid, axis and title colors, as well as left, center, and right titles can now be customized in W-Edit. Use **Setup > Chart Styles** to change the default settings for all charts. Right click on a chart and choose Chart Properties to change the settings for specific chart. Selection color of cursors, markers and labels can also be set in **Setup > Selection Style**.

Save Image to Windows Metafile

- W-Edit can now save a chart image as a windows metafile. Use **File > Image**, and select Save to file or Copy to Clipboard.

Import/Export traces from/to a file or clipboard

- Traces can now be defined by reading data from a file or from the clipboard. To define a trace from a file, use **trace define -file fileName -name traceName**, to define a trace from data in the clipboard, use **trace define -clipboard -name traceName**.
- A new function has been added to allow chart data to be copied to the Windows clipboard, from which it can be pasted to an external programs such as Excel. A new item, **Copy Data to Clipboard** has been added to the chart context sensitive menu. When executed, it runs the command "calc -clipboard", which will operate when there is a singly-selected curve. The calc -clipboard command can also be issued directly from the command line.

Other Improvements

- Three new workspace commands have been created, workspace getactive -simversion, workspace getactive -simfile, and workspace getactive -simdate, to get the T-Spice version used to create the active data, the Spice filename corresponding to the active data, and the date the active data was created.
- The calc command can now operate without specifying the trace name when there is a single curve on a chart, or only one curve selected on a chart.
- Fixed cursor behavior when multiple plots are present.

Note on Trace Style Settings

- Setup > Trace Styles settings written by W-Edit v15.02 and earlier will no longer be compatible with v15.10 as the **setup chart** tcl command has become obsolete, in favor of the new **setup chartstyles** command.

Bug Fixes

- When a simulation has more than 50 .probe and .print statements, W-Edit no longer presents a dialog saying ""Stopped adding trace expressions at 50", but simply logs a message to the log window.
- Traces with undefined or infinite values can now be rendered in W-Edit by skipping those values.
- Improved performance loading and displaying DC sweep traces with very large numbers of data points.
- Several bug fixes in printing have been made.

What's New in L-Edit Pro v15.10

HiPer DevGen

- The resistor generator in HiPer DevGen now has the ability to create resistor arrays. SDL is now able recognize resistors in a netlist that have the same L and W and combine them into a single resistor array.
- Keep-Out layers for each metal layer are now included in the HiPer DevGen Setup Process.

TCL Support

- TCL can now be used in L-Edit, either on the command line or in T-Cells. To see the list of available TCL commands, enter "help" on the command line. In a T-Cell, select Code Language TCL to use TCL.

Wire Drawing with Vias

- Manual routing is now much faster with improved via placement tools. While drawing a wire, the Draw Contact Down key "[" and Draw Contact Up key "]" now end a wire, place a contact, and start a new wire, all with one key stroke.

Snapping to Intersections

- A new snapping mode is available to snap to intersections. Snapping to intersections operates on all objects (boxes, polygons, wires, circles) and works through hierarchy.

Other Improvements

- When a net or instance is selected in the SDL Navigator in L-Edit, you can now highlight that net or instance in S-Edit. Use the SDL context menu.
- When closing a file with unsaved changes, an dialog is presented asking to save the file. Now an additional dialog is presented giving the opportunity to save changes if the first dialog is dismissed.
- A new **Vias** tab is added to **Setup Design** which lets one setup via cells, and the layers they connect. This tab provides the list of vias to be used when placing vias while drawing a wire using the Draw Contact Down key "[" and Draw Contact Up key "]", and is also used by SDL Automatic Router for the list of candidate vias cells. Contact created with the **Draw > Contacts > Define Contact or Guardring** are automatically added to this tab.

Bug Fixes

- Fixed a problem where Node Highlighting would not work in certain conditions when a derived layers was used in the setup.
- The DRC rules, guard rings and contact cells are now read in when performing an Import Laker Setup.
- Fixed crash in Replace Setup when file path/name was longer than 40 characters.
- Slow response when displaying "Bottom up – all cells" in Design Navigator has been fixed.
- Performance of insertion of error objects on layout has been improved.
- Fixed crash in LVS if one of the input file is missing when running in batch mode.
- File > Export Batch File... now exports "lvs64" instead of "lvs" when running in Win64.
- Fixed All-Angle Slice problem when slicing at 45 degrees.
- Snap to edge can now snap to an edge of a box that is not on the mouse snap grid.
- Fixed a snapping problem when using Force Move (Alt-M) with object snapping to move a polygon and place one of it's vertices on the vertex of another polygon.
- Fixed a bug in GDS export where the toplevel cell could sometimes be missing for certain number of cells in the design.

What's New in HiPer Verify v15.10

Improved Extract performance

- Performance of Extract is significantly improved for certain designs using an EXTENT calculation.

New Commands

- The BEVEL option in the Calibre SIZE command is now supported.
- The list of #DEFINES that are set is now listed in the Verify Summary Report.

Bug Fixes

- Fixed a problem where diodes were being incorrectly extracted.
- Fixed a problem where pin names were compared case sensitively, but should have been compared case insensitively.
- Fixed incorrect L and W values when using the BY SHAPE device option in Extract, when source and drain are connected.
- When VIRTUAL CONNECT COLON is used, extract will now correctly remove the characters after and including the colon when forming the net name.

Tanner Tools Version 15.02

What's New in S-Edit v15.02

- When exporting Spice, quoting of expressions containing spaces is now handled correctly.

What's New in T-Spice v15.02

- 31281 Fixed noise plot items - inoise(m), inoise(db), inoise(tot), etc.
- 31366 PWL sources can now accept a single point in the pwl vector.

What's New in W-Edit v15.02

- W-Edit now loads tsim files correctly when the simulation results folder has Japanese characters.
- In Japanese UI, changing Spice Simulation > General > Show Waveforms to "{Don't show}" no longer gives an error.

What's New in L-Edit Pro v15.02

- When exporting GDSII with the option Overwrite object data type with layer data type" set, a warning is now issued if the layer data type is blank.
- When importing a Spice netlist into SDL, SDL now correctly instances X-Ref cells containing T-Cells.

What's New in HiPer Verify v15.02

- VIRTUAL CONNECT COLON is now supported in HiPer Extract.

Tanner Tools Version 15.01

What's New in S-Edit v15.01

- On Verilog import S-Edit now issues a warning when case-insensitive name collisions occur, for nets and for instances.
- A problem with corruption of instance names on Verilog export is fixed.
- A problem where instances would show some parts as selected is fixed.
- In Setup Simulation, a new sweep type named <disabled> has been added for DC and Parametric Sweeps, to enable a particular sweep to be disabled.
- Custom Settings in **Setup Technology** can now be saved correctly into the project folder.
- S-Edit will now check if a design has been modified by another user prior to saving, and will give a warning and not save if the design has been modified.
- Added an option "Exclude instance locations" in Spice Export to suppress writing of the instance locations.
- S-Edit can now print to printers other than the default printer.
- Current probing on subcircuits now shows Mag and Phase, same as when probing primitive devices.
- Fixed problem where Design Check was reporting an incorrect number of errors and warnings.
- Fixed problem with the Display.WhenNotEvaluated property to correctly display current annotations.
- Fixed problem where print with Selected Design/Libraries is printing out duplicates causing more printed pages than necessary.
- Fixed problems with Jump > Device in Schematic and Jump > Net in Schematic, when jumping from devices and nets in a netlist to schematic.
- Fixed incorrect results in Spice export in certain circumstances when using net caps.
- Added a new checkbox to Open Design, called "Open design for writing, and libraries read-only". Here "Open as read-only" does not mean "don't write", rather it means "do not grab a lock (i.e. a write-reservation)".

What's New in T-Spice v15.01

- Added support for encryption of T-Spice netlists using .protect and .unprotect commands combined with the **File > Encrypt...** command.
- Corrected external C device terminal connections error test, which was sometimes issuing incorrect error messages.
- The numerical format of .measure command outputs are now controlled by the **ingold** option: 0=engineering notation and 1=scientific notation.
- Added support for g element (VCCS) and h element (CCCS) M multiplicity parameter, which inherits through the subcircuit hierarchy.
- Limit the amount of repeated error message printouts, using option MAXMSG to set the limit.
- Improved fault tolerance for controlled-source expressions that may result in a 'divide by zero' error.
- Corrected the .measure **pp** peak-to-peak calculation
- Added limits to the Monte Carlo log messages, and send output to the new *.monte output file.
- Changed the default setting for **.option csv=[012]** to 0, to disable generating the *.csv comma separated value file.
- Corrected a bug where node names containing a colon were truncated to just those characters following the colon.

- Diagnosed problems compiling Verilog-A code on a network drive: Windows UAC (User Account Control) must be disabled. Please contact support for further information if you are unable to compile modules that are stored in network files.
- Ensured that the plot command `i(devicename)` is equivalent to `i1(devicename)` for all devices and all output commands (`.print`, `.measure`, `.assert`, etc.)
- Modified the syntax for conditional statements in expressions (`c ? a : b`) to not necessarily require spaces surrounding the `?` and `:` characters.
- Corrected some circumstances where a column 1 '+' continuation character caused errors within expressions.
- T-Spice now treats "\$" as an end of line comment in P-Spice mode.
- Various performance improvements relative to T-Spice v15.00

What's New in W-Edit v15.01

- Cross probing of AC simulations now works correctly.
- Added a new tcl command `measure cursor -cursor xxx` to return the x position of vertical cursor named xxx or the y position of a horizontal cursor, as a real number.
- Fixed problem where `.alter` variations were being combined into a single `.alter` in the variations browser.
- MeasureAt now returns the correct result.

What's New in L-Edit Pro v15.01

- Fixed crash clicking Cell Width button when multiple instances selected.
- `position`, `moveorigin`, `locate`, `layer`, `save`, `database cells`, `database xreffiles`, `database layers`, `property get`, `property set`, `property delete` now operate in T-Cells. Previously, they only operated on the visible cell.
- Auto-panning now works correctly for all objects, regardless of mouse button state.
- **Add selection flyline** now works with HiPer DevGen T-Cells.
- Fixed "Out of memory" error in node highlighting by handling circles correctly.
- Importing a netlist in SDL now first checks the Additional XRef Libraries in the SDL Import netlist dialog, then checks the XRef files in Setup > Design > XRef files, in the order they are listed.
- Note: If problems occur in writing the user `ledit.ini` file, as a work around on Windows Vista and Windows 7 one can turn off User Account Control (UAC), or move the file out of the programs folder to a data folder.

DRC

- The **Ignore Acute Angles** option now works correctly in L-Edit/DRC.

What's New in HiPer Verify v15.01

- Problem loading DRC results when multiple rule files are run is fixed.
- Running a single rule now only computes connectivity if necessary. In previous versions, when DRC INCREMENTAL CONNECT was set to YES, then connectivity would always be computed when running a single rule.
- False errors in Net Area Ratio are fixed.
- Problem in calculation of `ABUT ==90` option in DRC rules is fixed.
- Fixed **Jump to DRC Rule** for SCONNECT violations.
- Fixed problem parsing "Inside of Layer" option of RECTANGLES operation.
- Improvements are made in the removal of duplicate operations in command files.
- Improved parsing of Calibre command files to recognize new commands.

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What's New in S-Edit v15.00

Spice and Verilog-A Text Views

- S-Edit now supports Spice and Verilog-A text views. Any combination of i) schematic, ii) Spice, and iii) Verilog-A view may be saved for a cell. The view that is used when simulating is given by a priority list of view types and view names defined in the Hierarchy Priority tab of the Setup Simulation dialog. A similar list is on the Export Spice dialog for use when exporting Spice.

Spice Command Tool

- The Spice Command Tool for inserting new Spice commands is now available in the **Additional Spice Commands** page of the **Setup Simulation** dialog. The **Insert Command...** button is used to invoke the wizard.

Model Parameter Listings

- A table showing all the models supported in T-Spice is now available in S-Edit via the **Help > Models Supported by T-Spice...** menu. A table showing the models used in the libraries specified for the current design is available via **Tools > T-Spice Library Models**, and a table showing the device parameters for all devices in the design is available via **Tools > T-Spice Device Parameters...**. The **Help > Models Supported by T-Spice** table shows default values for all models and devices, whereas the **Tools** menu shows tables with the actual models and device values to be used in the simulation of the current design.

Design Checks

- Performance of design checks has been significantly improved. A limit of 20 errors are reported for each design rule.
- A new design check for checking overlapping wires has been added.
- The default severity of "illegal connectivity" design checks, such as connecting buses of different widths, is now Error instead of Warning.
- The design check for overlapping instances now ignores symbols that do not have any ports. This prevents the design check from flagging frame instances, which overlap the entire schematic.
- Design check now performs cell name checks in a case insensitive manner. Cell names in different libraries with same name but different case will now issue a warning/error.

Bug Fixes

- Performance of Push and Pop context is significantly improved.
- Design checks now properly identifies the case when two cells with same name are instanced from different libraries.
- Fixed problem when importing an EDIF schematic file created in S-Edit, the option "Overwrite existing views" did not work properly.
- S-Edit has a new Simulation Setup option, "Keep all simulation results". When True, a time stamp is appended to the Simulation Results folder, so each simulation is saved in a unique folder. When False, prior results are overwritten.

- Fixed problem where Verilog import would have missing pins when a module definition contains a port, but does not declare the port in the module's contents. These ports will now be declared as type "other" and a warning will be issued.
- Verilog import now imports parameters.
- Ports containing buses with {} brackets now import properly.
- Verilog Import dialog no longer reverts the TieHigh cell: value to TieHigh even when something else is specified.
- Fixed a problem where Property set would apply to selections that were not on the active page.
- Selecting properties on symbols will now select the property that is clicked on. Using the left mouse button will cycle through overlapping properties, allowing one to select difficult to select properties.
- Fixed a problem where a box width could not be changed to be greater than 66 inches.
- An option "Exclude simulator commands" is added to the Spice Export dialog to suppress simulation setup commands during Spice export.
- "New properties \${PageNumber} and \${Pages} have been added. \${PageNumber} evaluates to the 1-based index of the page that contains the instance. \${Pages} evaluates to the total number of pages in the schematic view that contains the instance.
- Zoom to selection now works correctly on highlighted nets
- ORCAD EDIF files may now be imported and the netlisting commands are correctly translated for exporting Spice.
- "Author (renamed from "Creator"), Version, Modification Date ("Last Modified"), Info and Organization and RevisionCount are now included as column choices in the View Navigator.
- Import of Cadence EDIF files now reads callbacks from the cdf file and places the function name and parameters on the property. A tcl file with stubs for the functions is created for the user to provide the content of the tcl function.
- Problems importing EDIF written by the Gateway Schematic Editor are fixed.
- Tcl scripts saved from S-Edit and placed in the user preferences startup folder will now properly load on program startup.
- Exported netlists are now sorted within each sort order block. The sort first sorts the alphabetic characters and then sorts any numbers in the name as a number. For example, the sort will produce C1, C2, C10, C11, whereas a normal alphabetical sort would be C1, C10, C11, C2.
- Printing will now print all pages of a schematic view, rather than just the first.
- In Setup SPICE Simulation, the Verilog search path is now saved.
- When separated by a space instead of a comma, negative values in temperature sweeps were being evaluated as an expression. The description field has been enhanced with: "Use commas to separate negative numbers or expressions"
- Annotations on schematic are now updated automatically after each simulation. It is no longer required to turn off then back on annotations to update after a simulation.
- The InstanceName property on a symbol can now be used as a prefix to use for the instance name when creating a new instance. If InstanceName is "M" then instances will be named M_1, M_2, etc. If InstanceName is blank, then the cell name is used.

Known Issue

- When v15.00 is installed over v14.13, hotkeys don't appear for all items in the Edit menu when a text document is active, although they do function correctly. A workaround is to open the Customize dialog on the toolbar context menu, go to the Keyboard tab, and click the Reset All button. This will restore the shortcuts to the menu, but will undo any custom keyboard shortcuts you have configured.

What's New in T-Spice v15.00

T-Spice Model Parameter Listings

- A table showing all the models supported in T-Spice is now available in S-Edit via the **Help > Models Supported by T-Spice...** menu. The table shows the parameters and their default values for all models supported by T-Spice.

Miscellaneous

- VBIC 3 terminal devices are now supported; 4 terminal VBICs remain as before.
- The .assert command can now be used to monitor Verilog-A device terminal currents.
- Binned model naming convention, where the name consists of a trailing period and number (e.g. nch.1), now additionally allows a trailing period without a number (nch.).
- .print output is now written to a CSV (comma-separated value) file as well as the binary database. CSV files can be easily loaded into spreadsheets and other applications. CSV output is controlled with the new option csv=[0 | 1 | 2], 0: disable, 1: store .print outputs (default), 2: store .print and .probe outputs.
- The TC1 and TC2 parameters are now supported for all types of capacitors and resistors (voltage-controlled, polynomial, etc.)

What's New in W-Edit v15.00

Completely New W-Edit

W-Edit has been completely rewritten for Tanner Tools v15, and features significant improvements over the previous version.

- **Waveform Calculator:** W-Edit v15 provides a calculator for creating and evaluating expressions involving traces or measurements. The calculator provides trig, and hyperbolic trig functions, exponentiation and logarithmic functions, complex number functions, and mean, median, and standard deviation functions. The calculator provides a platform for easily creating arithmetic traces.
- **Measurement Platform:** W-Edit v15 is not only a waveform viewer, but is an analysis platform featuring built in measurements that can be applied to selected traces. These include amax, amin, amplitude, average, baseline, compare, cross, delay, derivative, edgethreshold, error, falltime, frequency, integral, intersect, maximum, minimum, nextedge, nextextreme, nextpoint, overshoot, period, previousextreme, previouspoint, pulsewidth, risetime, rms, slewrate, smooth, topline, undershoot, window, xval, ymax, ymin, yval.
- **Arithmetic Traces:** W-Edit v15 supports an ability to create new traces from arithmetic expressions of other traces. Arithmetic traces can be used in expressions or other arithmetic traces. Arithmetic traces can be saved in the W-Edit chartbook.
- **Multiple Simulations:** W-Edit v15 supports loading and viewing of multiple simulations. Results of multiple simulations can be plotted together for comparison and measurements.
- **Programmable:** W-Edit v15 is fully programmable with tcl, allowing the user to write scripts to automate results analysis.
- **Performance:** W-Edit v15 is a high performance waveform viewer able to handle your largest datafiles with ease. The trace navigator is able to display traces in a flat or hierarchical view, with filters including wildcards and regular expressions.
- **Chartbooks:** All configuration aspects of a chart, including arithmetic traces, can be saved to a chartbook for later display.

- **Intuitive GUI:** Drag-and-drop traces onto a chart. Easily view results of parameter sweeps on a single plot, and show/hide results of selected sweeps. Take measurements with multiple cursors.
- **Backward Compatibility:** v14 simulation databases can be converted to v15 format using Wavetool.

What's New in L-Edit Pro v15.00

Dev-Gen

- Dev-Gen, the device generators for mosfets, resistors, capacitors, diodes, and inductors has been rewritten with an improved setup and now uses T-Cells, rather than simply placing polygons. As T-Cells, the parameters of devices placed by Dev-Gen can now be edited.

HiPer Dev-Gen

- HiPer Dev-Gen is a new module of advanced layout generation macros for current mirrors and differential pairs, providing substantial time savings for laying out these complex devices. Mosfets, resistors, and capacitors are also included in HiPer Dev-Gen. HiPer Dev-Gen macros can be instanced as T-Cells in the same manner as standard Dev-Gen T-Cells. Schematic Driven Layout (SDL) is also able to automatically recognize primitive transistors configured as current mirrors and differential pairs, and to place the appropriate T-Cell for that device.

Import Calibre into Interactive DRC

- Calibre® rule files can now be imported into online DRC.

SDL Placement

- SDL now uses the schematic placement as a guideline for placement of instances when importing a netlist. This is an improvement over the previous behavior of simply stacking instances in a column.

SDL Automatic Routing

- The SDL automatic router now supports single layer routing. This is most successfully used in a river routing situation in which one is routing a bus with no crossover of nets, and all pins are on the desired layer, although breakouts are allowed to route from pins that are not on the target layer.
- The SDL router now supports double vias. Create a cell that has a double via in it, then use that cell as your via cell in SDL Router setup.

Extract

- Extract is now able to label devices by placing port objects at the location of each device. The text of the port is the name of the device.
- Extract now writes device and node counts into the netlist. For a hierarchical netlist, device and node counts are written for each subcircuit, and for a flat netlist the total node and element count is written.
- A new option, BY_NET has been added to the device definition in the standard Extract definition file. This option counts multiple pins of the same layer that are connected to the same device as a single pin of the device.

Bug Fixes

- Interactive DRC now works correctly with multi segment wires.
- Two command-line options are added to L-Edit, S-Edit and W-Edit:
 - t <filename> --- causes that tcl file to be 'source'd
 - T <commandname> --- executes the Tcl command <commandname>
- DXF import/export can now handle the ^ character.
- CTRL+ drag box can now select both ends of a wire
- Splines are now imported in DXF. They are sampled as 20-sided polylines.
- L-Edit no longer crashes when dragging a text file onto the Design navigator.
- GDSII Export with lower case option no longer appends _1 to the cell name.
- L-Edit-64 is now able to save TDB files greater than 2GB.
- Fixed a problem where updating the source code of a T-Cell in an x-Ref cell, and then updating the x-Ref T-Cell, the links to the x-Ref cell would become broken.
- When layers are hidden, running Extract will now bring up a dialog asking if geometry on the hidden layers should be ignored, or shown and used.
- Fixed problems when parenthesis was used in recognition layer names in extract definition file.
- Fixed problem where end of line comment using # would comment out entire line in EXT file.
- Fixed problem where ascii control characters in the Setup DRC Standard Ruleset dialog would cause DRC to not report any violations

What's New in HiPer Verify v15.00

- The Verification Error Navigator is now able to highlight multiple rules at the same time. Click on a rule name to highlight all violations of a rule in the active cell. When violations are sorted by cell first, click on a cell name to highlight all violations of all rules in the selected cell.

Calibre® Compatible Format

- WITH NEIGHBOR is now supported.
- The REGION CENTERLINE option for INT, EXT, and ENC rules is now supported.
- Netlist Comment Coded Substrate is now supported. If Netlist Comment Coded Substrate is set to YES extract will write three pin resistors, diodes and capacitors as two pin devices with third pin in comments. In set to NO extract will write these devices as a primitive subcircuit.
-

Bug Fixes

- EXPAND CELL now correctly expands instances of specified cells one level into the cell in which such instances are placed. Previously EXPAND CELL would completely flatten instances of specified cells. EXPAND CELL also now will match to T-Cells, which have a suffix of _AUTO*, and x-Ref Cells, which have a suffix of :LibraryName.
- Fixed checking of the OVERLAP option of ENC command, to make sure that polygons are properly overlapping and not just coincident before performing overlap check.
- Fixed ENC with SINGULAR option which would sometimes give false errors between abutting cells of a hierarchical layout
- Implemented special case handling of ABUT == 0 for ENC, EXT, and INT commands. If the abut constraint includes zero in its range then, for ENC, any edges that are coincident inside are also output, and for EXT and INT, any edges that are coincident outside are also output.
- The OFFGRID command is now able to use an expression in the layer parameter, for example, OFFGRID (A not B) 5

- The SNAP command is now able to use an expression in the layer parameter.
- Fixed a problem where WITH WIDTH command was not considering very thin 45 degree polygons.
- Fixed a problem where expressions inside a NET AREA RATIO command inside a DRC rule were incorrect.
- Fixed problem with rule names containing an "&"
- Fixed a problem when a DRC rule is written using variables in rule comment, the Verification Error Navigator window would only substitutes in the first parameter.
- Extract is now able to label devices by placing port objects at the location of each device. The text of the port is the name of the device.
- Extract now writes device and node counts into the netlist. For a hierarchical netlist, device and node counts are written for each subcircuit, and for a flat netlist the total node and element count is written.
- Fixed problem where pins of a device were incorrectly shorted.
- False SCONNECT warnings are no longer reported
- Problems reading in verification errors into the Error Navigator after Extract have been fixed.
- A problem in which the collector and emitter of a BJT were getting shorted has been fixed.
- Fixed crash caused by mismatching case in layer names.
- Fixed syntax checking problem that would cause L-Edit to hang.
- Fixed a problem where a device was identified as a bad device in hierarchical layout, but would be recognized properly when flattened.
- Fixed problem that caused \$\$ TwoLayerPerimeterCalculator: internal error #3
- Fixed problems in hierarchical extraction related to pushing down of devices.

What's New in HiPer PX v15.00

- There are no new features in HiPer PX v15.00.

Additional Information

Supported System Requirements

Microsoft® Windows XP, Windows Vista™ or Windows 7.
Intel® Pentium® 4 processor or Pentium 4 equivalent with SSE support
1 GB RAM
425 MB of available disk space with an additional 100 MB during installation
A video card with at least 64 MB of memory
3 button mouse

Recommended System Requirements

Microsoft® Windows 7 64-bit
Dual Core Intel® Xeon® 2.66 GHz or better processor for desktops
Intel® Core™ 2 Duo 2.00 GHz or better processor for laptops
It is recommended to get a computer with at least 2 cores and the fastest processor speed you can afford. Tanner Tools can take advantage of 2 cores/processors but not more. It is also recommended to get the fastest RAM you can afford.
4 GB RAM (more memory recommended if you use HiPer Verify)
1 GB of available disk space with an additional 100 MB during installation
A video card with at least 256 MB of dedicated memory
Microsoft® Intellimouse
1280 x1024 Resolution - True Color (24-bit)

Installation

Install Tanner Tools from the Windows operating system. To begin, insert the distribution CD into your CD-ROM drive. The setup program should start automatically; if it does not, then you should navigate to the main CD directory from a file browser window, and double click SETUP.EXE to run setup. The Tanner Tools setup program will provide information on how to proceed.

Administrator Privileges are required to install Tanner Tools v14. Power users are no longer able to install Tanner Tools, as they could in previous versions. On some Windows Vista machines, the following error will appear when installing, even if you are logged in as an administrator: "Error 1925. You do not have sufficient privileges to complete this installation for all users of the machine. Log on as an administrator and then retry this installation." If this occurs, the right-click on setup.exe on the installation CD and select option Run As Administrator. This will bring you Tanner Setup window and the installation will proceed.

Starting Tanner programs from the Windows Start menu, when logged in as a different user than the user who performed the installation, will sometimes result in a message from Windows requesting insertion of the installation CD. Inserting the CD and following the instructions will complete the installation for this user, and the message will not appear again. If you install just T-Spice and want to run Verilog-A, you must also install Minimalist GNU for Windows using Custom Installation.

Licensing

Tanner Tools is licensed software; to use the program, you must have a license from Tanner Research, Inc. Tanner Tools will verify the license either from License Server, installed on your company network, or from a hardware lock attached to your computer's parallel port. Tanner Tools is available in node- or network-locked licensing.

When using the **Interlink** or **LapLink** utilities over the same port as the Tanner Research **Sentinel C-Plus-B** hardware lock, the user must first remove the hardware lock from the parallel port. This must be done in order to keep the Sentinel C-Plus-B lock functional.

This version of Tanner Tools uses the SentinelLM version 7.3.0.6 License Server.

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