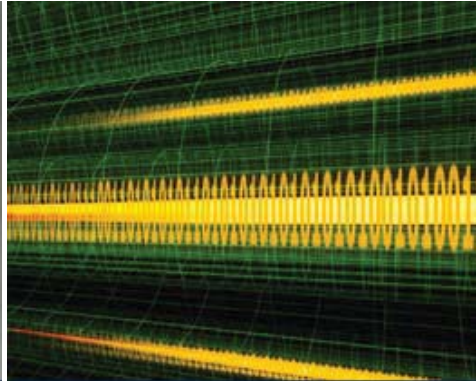


# Tanner EDA Today

Driving Analog Innovation



**From the Founder and CEO:  
Then and Now**



**What's New in Tanner  
Tools v15**



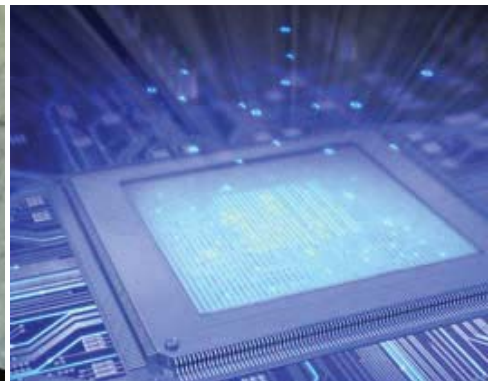
**FAE Focus:  
Karen Lujan, FAE Manager**



**Analog Insights:  
Layout is Becoming a Bottleneck**



**From the President:  
State of Analog**



**Tips & Tricks:  
From Karen Lujan**

## From the Founder and CEO: Then and Now



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Looking back at an early issue of a Tanner Research newsletter, "Tanner Tools News", from the mid-1990s, the theme at that time was growth, just as it is again now for Tanner EDA. At that time we were averaging 66% revenue growth per year, enjoying rapid growth as a small start-up. Fast-forward to current day, where we just closed our fiscal year 2010 as a record for the company, with fourth quarter revenue being the best in our history and May 2010 representing our strongest month ever!

Back in the mid-90s, the majority of our users were running on DOS, just beginning to switch over to Windows. Today, the majority of our users are on the Windows platform and we now offer the software for Linux as well. The mid-90s saw us touting version 1.0 for many of our products while most recently we [launched v15.02 of our full flow tool suite](#). Back then, we boasted an installed base of 3,000 seats while presently we have 33,000 worldwide. Steady, well-managed organic growth has brought us a long way and many things have changed, but we pledge to sustain the same core values that made us successful then and continue to do so now.

*“In 2010 we continue to stay on top of market trends and demands and drive analog innovation.”*

Tanner's first product, L-Edit, was launched in 1988 in response to a market need for cost-effective and easy-to-use EDA tools that would give engineers the performance and flexibility to handle complex design flows and help speed their design concept to silicon. Today we maintain a reputation for high quality, strong price performance, and the intuitiveness of our tools, allowing us to serve the analog design needs of the independent analog designer and the large corporation alike. And in 2010 we continue to stay on top of market trends and demands and to drive analog innovation.

At Tanner EDA, we promise the same thing today as we did back then, which is that we are dedicated to supporting, maintaining, and enhancing the products that you have purchased and to creating powerful new tools to aid in the complex IC design challenges that lay ahead. And, as we grow, we will continue to remain focused on doing so in a fiscally responsible manner.

- Dr. John Tanner, Founder & CEO

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## From the President: State of Analog

## Happenings @ Tanner

### TowerJazz Global Symposium

[October 26-28th](#) at TowerJazz's US Regional headquarters and fab site in Newport Beach, CA.

Tanner EDA is proud to be participating as a Silver Sponsor. We will be demonstrating our latest Analog IC tool flow, highlighting the foundry-approved Power Management PDK with TowerJazz.

### [View highlights from DAC 2010](#)

### [Enter the Tanner Press Room](#)

### [Learn more about our upcoming Webinars on Analog Layout Acceleration](#)

- September 14 at 7:00 am PDT
- September 21 at 2:00 pm PDT

### [Sign Up for Training at Tanner in Monrovia, CA](#)

## What's New in Tanner Tools: v15.02

Tanner's full-flow suite is now better than ever with the launch of v15.02 of our tools. We are currently working on version 15.10, with even more enhancements based on feedback from users. See for yourself how Tanner EDA is driving analog innovation.

### L-Edit Improvements

- TCL-based T-Cells
- Import Calibre rule sets into Interactive DRC into Interactive DRC

 [L-Edit Datasheet](#)

### Enhanced SDL and Module Generator

- Schematic-driven placement
  - Relative position and rotation taken from schematic symbol
- HiPer DevGen
  - Differential pairs, current mirrors, MOSFETs and resistors
- SDL Router improvements
  - Single-layer ("river") routing



Design complexity in the IC product development process is ever-increasing, as are shrinking process geometries. Meanwhile, pressures to speed up cycle times and to shorten overall time to market are mounting. The greatest value-add a tool vendor can offer to customers is to enable enhanced productivity and reliability and to speed the path to profitability. Tanner EDA has a 22-year history of providing this to our customers, who today include 33,000 seats in 67 countries.

Tanner EDA has consistently met the needs of our customers by, first and foremost, bringing to market high quality tools and, equally importantly, through our agility: the ability of our teams of application engineers and account managers to listen to customers and equip them to get their jobs done. As a result, Tanner EDA is driving analog innovation.

This is an exciting time for Tanner EDA both from a growth perspective, as mentioned by John Tanner, and from a product standpoint. April 2010 saw the release of v15 of our tools and the introduction of our new game-changing analog IC layout accelerator, [HiPer DevGen](#). In this first issue, the focus of our educational piece is on analog IC layout as a bottleneck in the design cycle, showing how attempts in the industry at automation have not gained traction and have been a disappointment. In the article we will touch on how Tanner EDA is addressing this challenge through acceleration rather than automation, with HiPer DevGen preserving the artistic nature of analog design and incorporating the value-add of the design engineer.

Analog IC layout acceleration with HiPer DevGen is a good topic focus for the reintroduction of our quarterly newsletter representing, as it does, how Tanner EDA has always managed to stay current on industry trends and challenges, customers' design and tool needs, as well as our continued commitment to innovation.

I hope you enjoy reading our industry topic selections and what's new at Tanner EDA quarterly in our newsletter.

- Greg Lebsack, President

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## Analog Insights: Layout is Becoming a Bottleneck

Despite many efforts to automate analog design and layout, these tasks remain primarily a full custom process with the result that analog is occupying a larger and larger portion of the total design cycle time. Efforts to automate analog design haven't been successful in the marketplace because the tools haven't been able to

- Double-via support

[SDL Datasheet](#)

### S-Edit Improvements

- Integrated Verilog-A and SPICE views
- User-defined netlisting priority of different views
- Spice Wizard added to "Additional SPICE Commands" dialog
- Model Explorer (S-Edit and T-Spice): view model and device parameters
  - Model names, versions, and information
  - Model parameters supplied in libraries
  - Device parameters supplied on instances
  - State variables calculated on instances

[S-Edit Datasheet](#)

### HiPer Verify Additions

- Additional commands
  - WITH NEIGHBOR is now supported
  - REGION CENTERLINE option for INT, EXT, ENC rules is now supported
- HiPer Extract enhancements
  - Labels devices by placing port objects
  - Device and node counts are now written in the netlist

[HiPer Verify Datasheet](#)

### All New W-Edit

- W-Edit is not just a simulation results viewer, but a Waveform Analysis Platform
- Built-in measurements
- Scripting

[Learn more about the all new W-Edit](#)

### HiPer DevGen Tool Offering

- T-Cell based device generation
- Differential Pairs
- Current Mirrors
- MOSFETs
- Resistors

equal the quality levels of custom design, are complex to set up and use, and are expensive.

Analog layout has traditionally been considered to be more challenging than digital layout. For example, it takes considerably more time to achieve a high level of expertise in analog layout as compared to the time required to master digital layout. So it comes as no surprise that digital design automation technology has advanced at a much faster pace than its analog counterpart. Since digital occupies the vast majority of most projects, design cycle times have trended downwards even as transistor counts have continued to increase geometrically.

Right now, most analog layout engineers use either a full custom approach -- drawing every polygon -- or use basic device generators provided by the foundry to create MOSFETs, capacitors, resistors, etc. The vast majority of layout engineers manually place these devices together to form basic analog structures such as current mirrors and differential pairs, which in turn are connected together to form the overall circuit. The quality of the resulting layout is obviously heavily dependent upon the expertise of the individual layout engineer.

The very long period of time required to develop expertise in analog layout means that skill levels vary widely among the members of the typical layout team. The lack of a consistent approach among members also drives up the time required for the review process and increases the risk of needing additional design spins. These problems appear most often in the more difficult areas of high speed, low noise, high precision analog design where device matching is critical to performance. Expertise in basic matching techniques can vary from engineer to engineer, which can in some cases lead to the chip failing. Layout engineers with the experience and knowledge to go beyond the basic techniques produce designs that are much more likely to work the first time, but such people are in short supply. A leading analog foundry recently cited matching issues as the single biggest cause of re-spins in their customer's designs.

[Learn more about the HiPer DevGen tool offering](#) and view our video demonstration

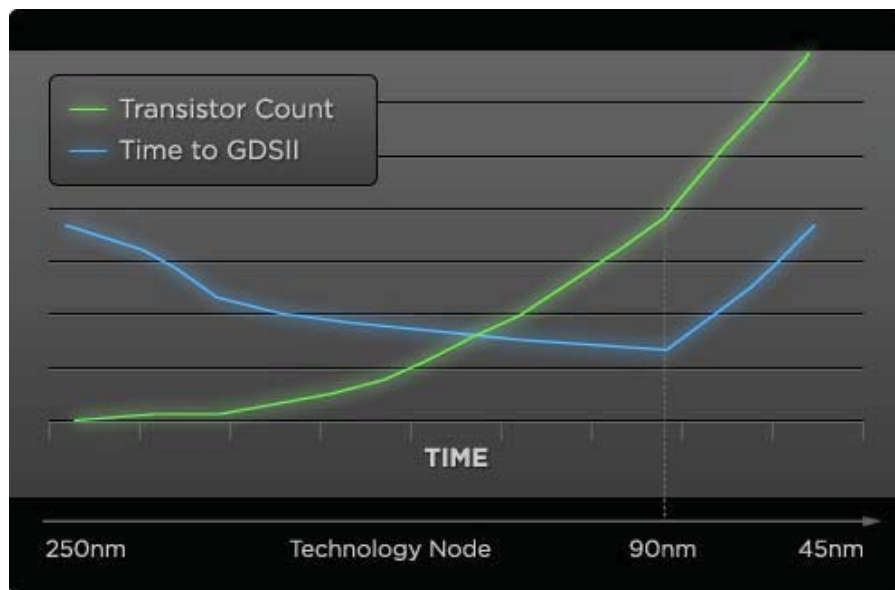


Figure 1: Transistor count vs. time to GDSII by Technology Node

As process technology moves deep into the nanometer realm, the impact of process variations and parasitic effects have caused the analog layout process to be highly iterative and time-consuming. Analog layouts often must be revised, re-simulated and the results evaluated over and over again to achieve a robust

solution. In a typical project, analog may occupy only a small portion of the silicon area but can consume a very large portion of the layout effort. As feature sizes are reduced, the time required for full custom analog layout is rising, with the result that many companies are seeing an increase in time-to-GDSII at nanometer technology nodes. Figure 1 shows data collected from a sampling of customers of IC Mask Design, a company that provides analog physical design services.

## **Existing analog automation solutions have not gained acceptance by users**

Large and small vendors offer varying approaches to analog automation, ranging from simple device generation tools to full-blown analog layout automation. One analog automation solution focuses on providing advanced editing features for creating and editing parameterized cells to expedite the process of creating matched structures. Another tool builds on the parameterized cell approach by adding many additional parameters and technology independence. Both operate only at the device level, so they do not address the layout of circuits and structures, which is not only the most time-consuming part of the analog layout process, but also the portion that is most prone to poor quality and inconsistency. Large amounts of time are required to generate individual structures by hand and the quality of the resulting layout varies depending upon the skill of the individual engineer.

Another analog layout solution attempts to completely automate the analog layout process. It provides a programming language that allows users to code their own physical cells and its placement engine generates the layout based on these cells. But the coding takes place at a high level that does not take into consideration the basic characteristics of the key building blocks and may not lay them out with the correct considerations. Users often find that the resulting designs do not compare in quality to a manually created layout. Yet another tool takes as input a set of design rules and then generates basic structures, which are also placed and routed. One weakness of this approach is that it applies global matching rules to the entire layout while skilled manual designers understand that a current mirror, for example, should not be laid out in the same way as a differential pair. One more obstacle to adoption is its list price, which is quoted at close to a million dollars for a single license.

## **Tanner EDA's HiPer DevGen (High Performance Device Generator) accelerates analog layout by automatically generating common structures**

A new approach is based on accelerating analog layout by generating primitives that are used over and over again such as current mirrors, differential pairs and resistor dividers. This approach creates these building blocks based on an understanding of the functional requirements that are needed to produce a high-quality layout. Rather than attempting to completely automate analog design, HiPer DevGen accelerates the most time-consuming aspects of the layout process to substantially reduce the amount of time required for analog layout while improving quality and design.

[Visit the Tanner EDA Web site to learn more about the HiPer DevGen product](#)

[Learn more about our upcoming Webinars on Analog Layout Acceleration](#)

## FAE Focus: Karen Lujan, FAE Manager



Karen brings a wealth of experience as a Sales Support Manager and Engineer, having served in both delivery and management roles prior to joining Tanner EDA in 2006. In addition to her technical support training, Karen is a Registered Patent Agent.

Karen holds a BS in Electrical Engineering and an MBA with a Technology Management focus.

In her free time, Karen enjoys ceramics and mud runs and just completed the Irvine Lake Mud Run in July.

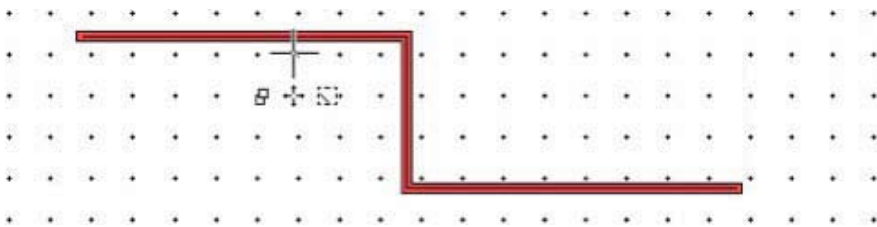
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## Tips & Tricks

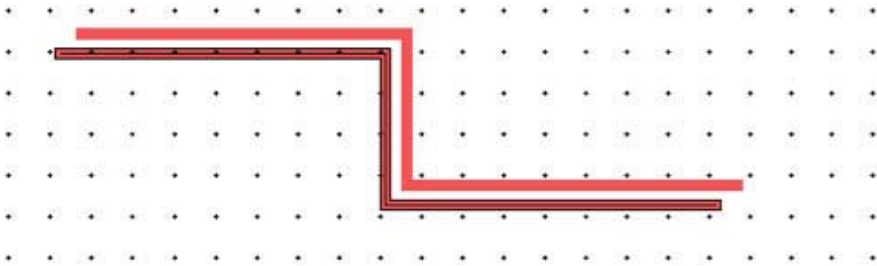
From Karen Lujan, FAE Manager and this quarter's FAE Focus:

### Tip 1 of 2: Creating Busses Quickly in L-Edit

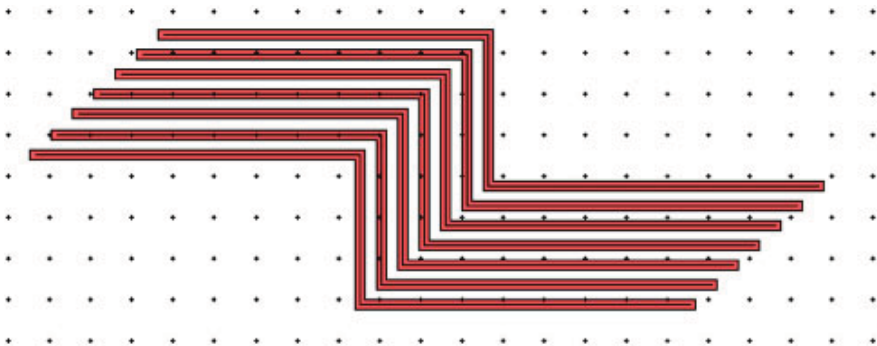
I love to show customers features that really speed up their productivity and that they may not have known were available in the tools. One of those features is how to quickly create a bus in L-Edit using a combination of the wire tool, duplication feature and the wire utilities. To create a bus, first select a layer from the Layer Palette (such as Poly) and select the wire tool by pressing **L** and draw a wire as shown below:



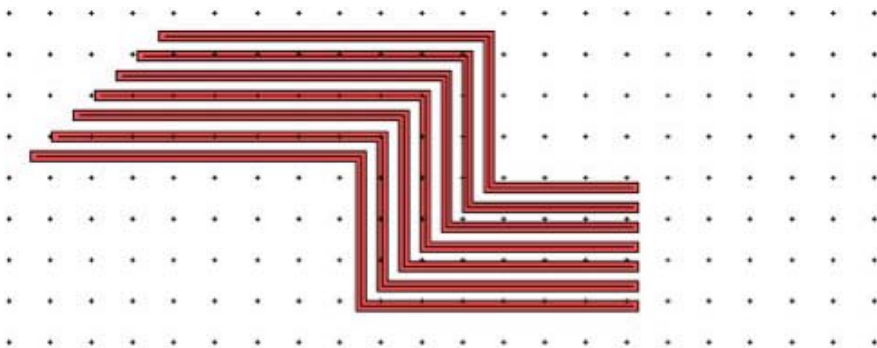
Next, duplicate the selected wire by pressing **CTRL + D** or **Edit > Duplicate**. This will create a duplicate wire directly on top of the original wire. Using your Middle-Mouse-Button, drag the duplicate wire away and space it the desired distance from the original wire as shown:



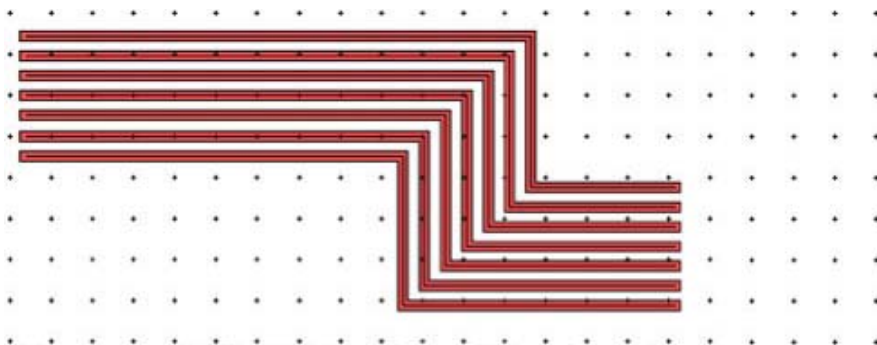
Press **CTRL + D** or **Edit > Duplicate** again to create yet another duplicate of the original wire. Notice that each duplicate now uses the same spacing you used from the original wire! Create as many wires as you want by repeating the **CTRL + D / Edit > Duplicate**. Select all the wires by pressing **CTRL + A / Edit > Select All**, or dragging around them using your Right-Mouse-Button. You should get something that looks like the following:



Press the **E** or select **Draw > Wire Utilities > Extend** to extend or truncate all the selected wires to a common vertical point as shown below:



Do the same on the other side of the wires using **E / Draw > Wire Utilities > Extend**



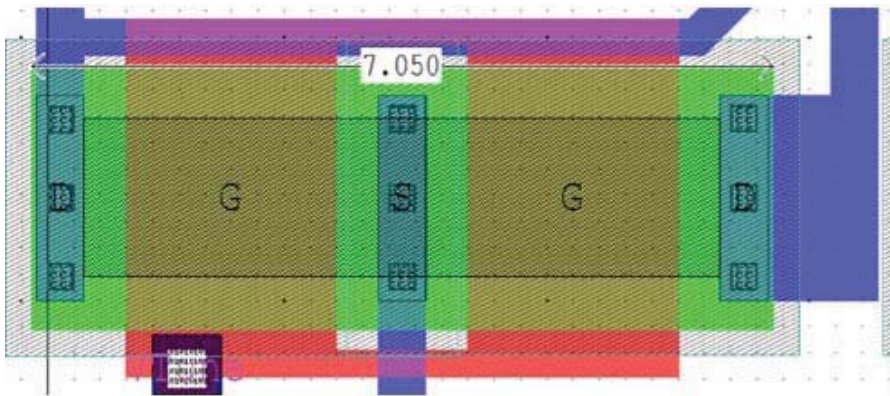
## Tip 2 of 2: Using Temporary Rulers in L-Edit

Many customers know how to use the permanent rulers that are located using the drawing icons but may not know about the option to create temporary

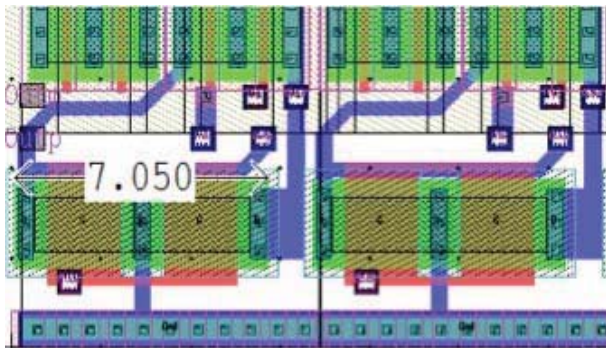


rulers to measure objects in their layout. Permanent rulers are placed in the layout using a specific layer from the layer palette or on a special “ruler” layer and stay on the layout until they are deleted just like other drawn objects. This is very useful for documentation purposes but you may not always want to have the ruler appear on the layout. Temporary rulers are available in L-Edit starting in v14.10 and higher. Temporary rulers can be placed, toggled on and off, or cleared with the click of a button.



A new temporary ruler may be drawn by pressing the **T** key or **Draw > Temporary Ruler** and then moving the mouse and pressing the Left-Mouse-Button to end and place the ruler. You can use this in conjunction with Object Snapping to achieve precision in the start and stop of the ruler. For example, below I have measured the length of the active region of this set of NMOS transistors:



A nice feature when using temporary rulers is that the text showing the distance will rescale depending on the zoom level you are at in the layout. This allows you to zoom in and out and still read the distance easily, as shown below when zoomed out on the same devices as above:

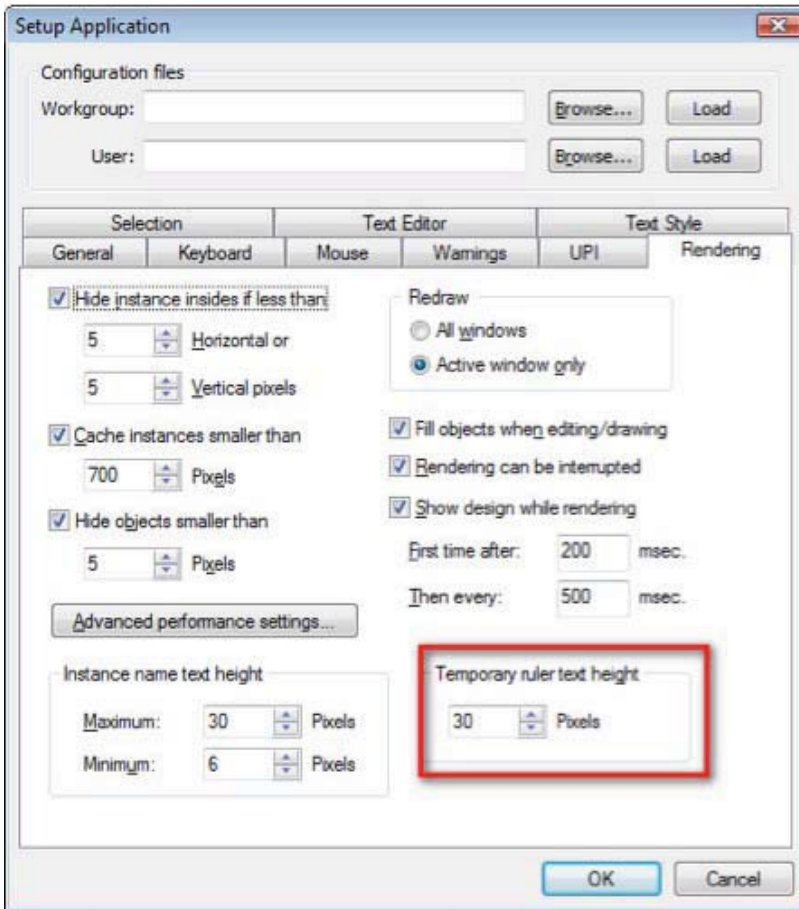


You can even start a temporary ruler while in the middle of drawing an object and the ruler will start wherever your cursor is located. Pressing the Right-Mouse-Button or pressing ESC during the drawing of a temporary ruler will erase the ruler.

Temporary rulers that have been placed may be hidden / toggled on-and-off by pressing the Toggle Markers icon  on the Node Highlighting, Verification Error Navigator, or SDL Navigator Toolbars. When the icon is depressed, the temporary rulers will be hidden and when not depressed will be visible. You can also clear all temporary rulers by pressing the Clear Markers icon  located just to the right of the Toggle Markers icon.

The size of the text that appears for temporary rulers can be modified by selecting **Setup > Application** and selecting the **Rendering** Tab. Just change the

**Temporary ruler text height** setting in Pixels.



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